Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims

1-21. **Cancelled**

22. **(New)** Method of transferring ownership of a cache line between processors in a shared memory multi-processor computer system using a directory-based cache coherency scheme, the method comprising:

sending a request transaction for ownership of a cache line from a first processor to a memory unit,

determining from the memory unit a second processor having ownership of the requested cache line and sending a recall transaction to the second processor, and

sending the requested cache line with ownership directly from the second processor to the first processor in response to the recall transaction regardless of whether an unacknowledged return request was sent by the second processor.

23. **(New)** Method according to claim 22, further comprising sending a response transaction from the first processor to the memory unit to confirm receipt of the requested cache line by the first processor.

24. **(New)** Method according to claim 22, further comprising sending a response transaction from the second processor to the memory unit to confirm that the second processor has sent the requested cache line to the first processor.

25. **(New)** Method according to claim 24, wherein the response transaction from the second processor to the memory unit includes a copy of the data of the requested cache line.

26. **(New)** Method according to claim 24, wherein the response transaction from the second processor to the memory unit includes a copy of the data for the requested cache line only when the request for ownership of the cache line from the first processor does not include a guarantee that the first processor will make the requested cache line data available in response to a subsequent request for ownership of the cache line.

27. **(New)** Method according to claim 22, further comprising updating a tag in the memory unit to reflect transfer of ownership of the cache line to the first processor.

28. **(New)** Method of transferring a cache line between processors in a shared memory multi-processor computer system that uses a directory-based cache coherency scheme, comprising

sending a request transaction for ownership of a cache line from a first processor in an m^{th} cell to a memory unit in an n^{th} cell,

determining from the memory unit a second processor in a p^{th} cell having ownership of the requested cache line and sending a recall transaction to the second processor regardless of whether an unacknowledged return request was sent by the second processor,

sending the requested cache line with ownership directly from the second processor to the first processor in response to the recall transaction, and

sending a response transaction from the first processor to the memory unit to confirm receipt of the requested cache line by the first processor.

29. **(New)** Method according to claim 28, wherein $m = n = p$.

30. **(New)** Method according to claim 28, wherein $m = n$.

31. **(New)** Method according to claim 28, wherein $m = p$.

32. **(New)** Method according to claim 28, wherein $n = p$.

33. **(New)** Method according to claim 28, further comprising sending a response transaction from the second processor to the memory unit to confirm that the second processor has sent the requested cache line to the first processor.

34. **(New)** Method according to claim 33, wherein the response transaction from the second processor to the memory unit includes a copy of the data for the requested cache line.

35. **(New)** Method according to claim 33, wherein the response transaction from the second processor to the memory unit includes a copy of the data for the requested cache line only when the request for ownership of the cache line from the first processor does not include a guarantee that the first processor will make the requested cache line data available in response to a subsequent request for ownership of the cache line.

36. **(New)** Method according to claim 28, further comprising updating a tag in the memory unit to reflect transfer of ownership of the cache line to the first processor.

37. **(New)** Method of transferring ownership of a cache line between processors in a shared memory multi-processor computer system that uses a directory-based cache coherency scheme, comprising

sending a request transaction for ownership of a cache line from a first processor to a memory unit,

determining from the memory unit a second processor having ownership of the requested cache line and sending a recall transaction to the second processor,

sending the requested cache line with ownership directly from the second processor to the first processor in response to the recall transaction regardless of whether an unacknowledged return request was sent by the second processor,

sending a response transaction from the second processor to the memory unit to confirm that the second processor has sent the requested cache line to the first processor, together with a copy of the data for the requested cache line,

sending a response transaction from the first processor to the memory unit to confirm receipt of the requested cache line by the first processor, and

updating a tag in the memory unit to reflect transfer of ownership of the cache line to the first processor.

38. **(New)** Apparatus for transferring ownership of a cache line between two processors in a multi-processor computer system using a directory-based cache coherency scheme having a shared memory unit, the apparatus comprising:

a first transaction line for providing a request transaction for ownership of a cache line from a first processor to the shared memory unit,

a second transaction line for providing a recall transaction to a second processor having ownership of the requested cache line, determined by the shared memory unit,

a third transaction line for providing transfer of the requested cache line with ownership directly from the second processor to the first processor in response to the recall transaction regardless of whether an unacknowledged return request was sent by the second processor, and

a fourth transaction line for providing a response transaction from the first processor to the shared memory unit to confirm receipt of ownership of the requested cache line by the first processor.

39. **(New)** Apparatus according to claim 38, further comprising a fifth transaction line for providing a response transaction from the second processor to the memory unit to confirm transfer of the requested cache line from the second processor to the first processor.

40. **(New)** Apparatus according to claim 38, further comprising a fifth transaction line for providing a response transaction from the second processor to the memory unit to confirm transfer of the requested cache line from the second processor to the first processor together with a copy of the data for the requested cache line.